EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	22	(second near (organosilicate or OSG)) and ((Silicon near oxide) or SiO or "SiO.sub.2")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/02 07:52
L2	1216	(organosilicate or OSG or organo$6) and damascene	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/02 07:50
L3	2401	(fluorocarbon or fluorine or "CHF.sub. 3" or "CH.sub.2F.sub.2 or ""CH.sub. 3F"" or ""CF.sub.4"" or ""C.sub.2F.sub. 6") near8 (etch or etching or etchant or etched) near8 (trench or trenches or via or vias or hole or opening or openings)	US-PGPUB; USPAT; USOCR	OR	ON	2006/08/02 07:50
L4	134	L2 and L3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/02 07:50
L5	404964	(SiO or "SiO.sub.2" or "SiO.sub.x" or "SiO.sub.n" or (silicon near oxide))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/02 07:50
L6	110	L4 and L5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/02 07:50
L7	44	L6 and ((@ad<"20010202") or (@rlad<"20010202"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/02 07:50
L8	2	("6410437").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/02 07:50

EAST Search History

L9	5	("5817572" | "5970336" | "6030901" | "6072227" | "6168726").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/08/02 07:50

US006072227A

United States Patent [19]

Yau et al.

[11] Patent Number: 6,072,227

[45] Date of Patent: Jun. 6, 2000

[54] **LOW POWER METHOD OF DEPOSITING A LOW K DIELECTRIC WITH ORGANO SILANE**

[75] Inventors: **Wai-Fan Yau**, Mountain View; **David Cheung**, Foster City; **Shin-Puu Jeng**, Cupertino; **Kuowei Liu**, Santa Clara; **Yung-Cheng Yu**, San Jose, all of Calif.

[73] Assignee: **Applied Materials, Inc.**, Santa Clara, Calif.

[21] Appl. No.: **09/114,682**

[22] Filed: **Jul. 13, 1998**

Related U.S. Application Data

[63] Continuation of application No. 09/021,788, Feb. 11, 1998.

[51] **Int. Cl.**[7] **H01L 23/58**

[52] **U.S. Cl.** **257/642**; 257/635; 257/636; 257/640

[58] **Field of Search** 257/635, 636, 257/640, 642, 647, 648

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,789,648	12/1988	Chow et al.	437/225
4,798,629	1/1989	Wood et al.	106/287.16
4,828,880	5/1989	Jenkins et al.	427/167
4,973,511	11/1990	Farmer et al.	428/216
5,040,046	8/1991	Chhabra et al.	357/54
5,204,141	4/1993	Roberts et al.	427/255.3
5,246,887	9/1993	Yu	437/238
5,250,473	10/1993	Smits	437/238
5,364,666	11/1994	Williams et al.	427/579
5,465,680	11/1995	Loboda	117/84
5,494,712	2/1996	Hu et al.	427/489
5,508,368	4/1996	Knapp et al.	427/534
5,554,570	9/1996	Maeda et al. .	
5,563,105	10/1996	Dobuzinsky et al.	437/240
5,578,523	11/1996	Fiordalice et al.	437/190
5,593,741	1/1997	Ikeda	427/579
5,598,027	1/1997	Matsuura	257/635
5,618,619	4/1997	Petrmichl et al.	428/334
5,637,351	6/1997	O'Neal et al.	427/255.3
5,683,940	11/1997	Yahiro	437/195
5,693,563	12/1997	Teong	438/627
5,700,720	12/1997	Hashimoto	437/195
5,739,579	4/1998	Chiang et al.	257/635
5,753,564	5/1998	Fukada	437/238
5,789,319	8/1998	Havemann et al.	438/668
5,807,785	9/1998	Ravi	438/624
5,821,168	10/1998	Jain	438/692
5,834,162	11/1998	Malba	430/317
5,858,880	1/1999	Dobson et al.	438/758
5,888,593	3/1999	Petrmichl et al.	427/563
5,891,799	4/1999	Tsui	438/624

FOREIGN PATENT DOCUMENTS

0 469 926 A1	2/1992	European Pat. Off.	C08J 7/06
0 522 799 A2	1/1993	European Pat. Off.	H01L 21/90
0 711 817 A2	5/1996	European Pat. Off.	C09D 183/04
0721019A2	7/1996	European Pat. Off. .	
0 774 533 A1	5/1997	European Pat. Off. .	
0721019A3	7/1997	European Pat. Off. .	
19654737A1	7/1997	Germany .	
60-111480	6/1985	Japan .	
01050429	2/1989	Japan	H01L 21/318
05267480	10/1993	Japan	H01L 21/90
9-237785	9/1997	Japan .	

OTHER PUBLICATIONS

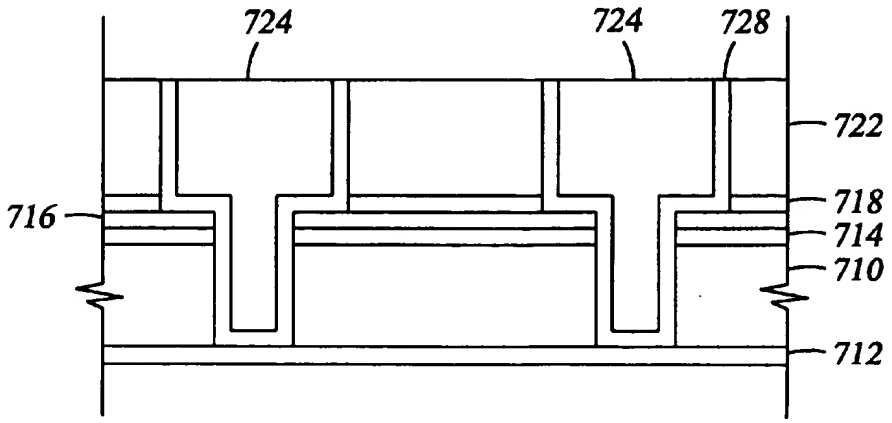
PCT International Search Report for PCT/US99/02903.

Primary Examiner—Mahshid Saadat
Assistant Examiner—Allan R. Wilson
Attorney, Agent, or Firm—Thomason, Moser & Patterson

[57] **ABSTRACT**

A method and apparatus for depositing a low dielectric constant film by reaction of an organo silane compound and an oxidizing gas at a low RF power level from 20–200 W. The oxidized organo silane film has excellent barrier properties for use as a liner or cap layer adjacent other dielectric layers. The oxidized organo silane film can also be used as an etch stop or an intermetal dielectric layer for fabricating dual damascene structures. The oxidized organo silane films also provide excellent adhesion between different dielectric layers. A preferred oxidized organo silane film is produced by reaction of methyl silane, CH_3SiH_3, and nitrous oxide, N_2O, at a pulsed RF power level from 50–200 W during 10–30% of the duty cycle.

26 Claims, 9 Drawing Sheets



US005817572A

United States Patent [19]

Chiang et al.

[11] Patent Number: 5,817,572

[45] Date of Patent: Oct. 6, 1998

[54] **METHOD FOR FORMING MULTILEVES INTERCONNECTIONS FOR SEMICONDUCTOR FABRICATION**

[75] Inventors: **Chien Chiang**, Fremont; **David B. Fraser**, Danville, both of Calif.

[73] Assignee: **Intel Corporation**, Santa Clara, Calif.

[21] Appl. No.: **768,790**

[22] Filed: **Dec. 18, 1996**

Related U.S. Application Data

[63] Continuation of Ser. No. 314,248, Sep. 28, 1994, abandoned, which is a continuation-in-part of Ser. No. 905,473, Jun. 29, 1992, Pat. No. 5,612,254.

[51] **Int. Cl.**[6] **H01L 21/44**

[52] **U.S. Cl.** **438/624**; 438/633; 438/637; 438/671; 438/945; 438/975

[58] **Field of Search** 438/624, 633, 438/637, 671, 945, 975, 700

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,844,831	10/1974	Cass et al. .
4,242,698	12/1980	Ghate et al. .
4,367,119	1/1983	Logan et al. .

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

9404603	10/1996	Rep. of Korea .
2211023	6/1989	United Kingdom .
2268329	1/1994	United Kingdom .
9110261	12/1990	WIPO .

OTHER PUBLICATIONS

S. Wolf "Silicon Processing for the VLSI Era: vol. 2" Lattice Press (Calif.) (1990) pp. 191 and 286.

J.J. Estabil, H.S. Rathore, & E.N. Levine, Electromigration Improvements With Titanium Underlay And Overlay In Al(Cu) Metallurgy, Jun. 11–12, 1991 VMIC Conference, pp. 424–248.

Eliot K. Broadbent, Janet M. Flanner, Wilbert G.M. Van Den Hoek, & I-Wen Huang Connick, "High–Density High–Reliability Tungsten Interconnection By Filled Interconnect Groove Metallization", IEEE Transactions On Electron Devices, vol. 35, No. 7, Jul. 1988, pp. 952–956.

"Process and Structure for Improved Electromigration Resistance," *IBM Technical Disclosure Bulletin*, vol. 32, No. 10B, pp. 112–113 (Mar. 1990).

"Lithographic Patterns with a Barrier Liner," *IBM Technical Disclosure Bulletin*, vol. 32, No. 10B, pp. 114–115 (Mar. 1990).

"High Stud–to–Line Contact Area in Damascene Metal Processing," *IBM Technical Disclosure Bulletin*, vol. 33, No. 1A, pp. 160–161 (Jun. 1990).

(List continued on next page.)

Primary Examiner—Caridad Everhart

Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] **ABSTRACT**

A method for forming interconnections for semiconductor fabrication and semiconductor devices have such interconnections are described. A first patterned dielectric layer is formed over a semiconductor substrate and has a first opening filled with conductive material. Another patterned dielectric layer is formed over the first dielectric layer and has a second opening over at least a portion of the conductive material. The first patterned dielectric layer may serve as an etch-stop in patterning the other patterned dielectric layer. Also, a dielectric etch-stop layer may be formed over the first patterned dielectric layer and over the conductive material before the other patterned dielectric layer has been formed. This dielectric etch-stop layer may serve as an etch-stop in patterning the other patterned dielectric layer. The second opening exposes a portion of the dielectric etch-stop layer. The exposed portion of the dielectric etch-stop layer is removed. The second opening is filled with conductive material.

37 Claims, 13 Drawing Sheets